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The Comparative Analysis of Power Optimization in Clustered Sleep Transistors

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Abstract
This paper concentrates on the various power reduction techniques for clustered sleep transistors and in particular leakage and dynamic power of the gated circuits published recently based on different logic styles. All the advantages and applications of the circuits have discussed with the relevant proofs of results and analytical models. All the circuits are designed and tested using spice simulation models and the screenshots of the different sleep transistor circuits based on Multi-threshold CMOS approach have depicted and its advantages over other methodologies have tested and its spice simulation results has presented with the required analytical model and the final layout of clustered sleep transistor has laid down.

Keywords: Dynamic power, Leakage power, MTCMOS, Low power, subthreshold values.

1. INTRODUCTION
From the last three decades CMOS devices have been scaled for achieving higher compact density, maximum performance and less power consumption. About every two years 30% of transistor delay decreasing with the advancements of the technology and thereby by increasing the microprocessors performance by twice that of earlier. And at the same time the supply voltage for the circuits have been maintain at the same level for meeting the lower power consumption. In order to achieve this higher performance factors the threshold voltage of the transistors should be

reduced to in proportionate to the other model parameters. The advancements of the portable electronic devices and high compaction of VLSI circuits, power dissipation give the major challenge to the designers. And also at the same time due to the advancements of the technological practice the increase of the leakage current is increasing due to the scale down of the supply voltage and also the threshold voltage.

In the deep submicron (DSM) regions, the reduction of dynamic power can be done with the reduction of supply voltages which in turn plays the important role for the reliability issues by using the advancements of the technology. The designer has to concentrate more about circuit performance as the reduction of supply voltages leads altering circuit's performance. And the mathematical notation for the subthreshold current can be denoted as follows.

$$I_{leakage} = I_0 e^{(V_{gs} - V_{th})/\eta V_T} \tag{1}$$

The subthreshold leakage current I_{leak} in sleep mode will be determined by the sleep transistor and is expressed as follows.

$$I_{leak} = \mu_n C_{ox} (W/L)_{sleep} e^{1.8} V_T^2 e^{\frac{V_{gs} - V_{tH}}{\eta V_T}} (1 - e^{\frac{-V_{ds}}{V_T}}) \tag{2}$$

Where μn is the N-mobility, Cox is the oxide capacitance, VtH is the high-threshold voltage (= 500 mV), VT is the thermal voltage = 26 mV, and n is the subthreshold swing parameter. The reduction of leakage power has achieved in the standby mode with the proposed methods [1]-[10]. By varying the substrate bias voltage the threshold voltage can be controlled which can be observed in Variable Threshold CMOS (VTCMOS) design.

The main advantage in this technique is low threshold voltage for all the transistors used for design. And it has the two different controlling aspects which are firstly, the delay variations can be minimized which cause compensations for fluctuations and secondly, reduction of the leakage current in the standby mode. These are the two things which need to be concentrating while implementing this design. Even though these two are crucial and plays the major advantages for design aspect but it has two disadvantages which cause the circuit reliability in dilemma. those are can be observed from its mathematical expression which is as leakage current is proportional to square root of the substrate voltage the resultant value would be about large change of effective values and final drawback is it require a triple-well structure and charge pump circuit for producing substrate voltage in the VTCMOS. These are the phenomenal causes for the VTCMOS circuit design.

And in contrast to the VTCMOS [4] technique, Multi voltage CMOS (MVCMOS) has LVT transistors where PMOS gates larger sleep mode voltages when compare to the NMOS gates which is different in the VTCMOS design. To reduce the drawbacks caused by these techniques virtual ground method has taken and by applying the clustering of the LVT transistors for reduction of the dynamic power and leakage power of the circuit which in turn reduce the leakage power of the sleep transistors has achieved. And the logic block diagram of the nMOS sleep transistor can be shown with the virtual ground and threshold voltage ranges in the Figure1.

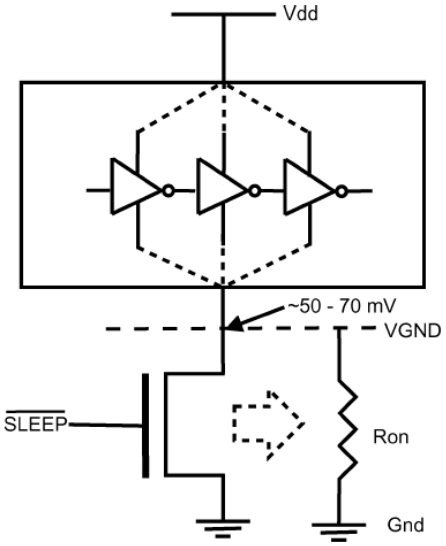

Figure 1. Logic block with an nMOS sleep transistor [6].

2. Leakage Reduction Techniques

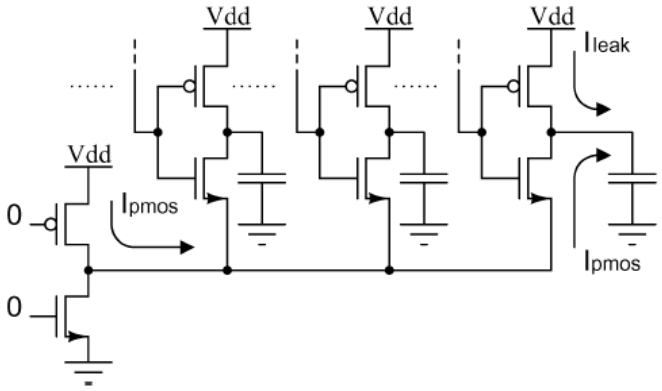

Figure 2. Charging of the zero output nodes with a pMOS pull-up.

The total power consumption can be computed in a CMOS circuit as the sum of dynamic power and the static power in the active mode operation. And due to the standby leakage current the power will be dissipated in the

standby mode. Due to the switching power during charging and discharging transitions of load capacitance and from the non zero rise and fall of input waveforms which leads to short circuit power consumption. These both the switching power and short circuit power combination is nothing but the dynamic power and where as the leakage current through each transistor is termed as static power of the CMOS circuit.

The dynamic power can be denoted in the mathematical notation as follows

$$P_D = \alpha f C V_{dd}^2 \tag{3}$$

$$P_{LEAK} = I_{LEAK} \cdot V_{dd} \tag{4}$$

3. Power Gating and Multi-Threshold CMOS

By turning off the supply voltage the leakage power can be reduced in the Standby mode which is the frequently used technique for reduction of the leakage power in the VLSI circuits. As shown in Figure 1 formation of virtual ground and virtual power can be formed with the single PMOS and NMOS transistors by connecting in series to the transistors of each logic block which can be done with the single transistor while doing the design. For this technique NMOS transistors are preferred because of their lower on resistance.

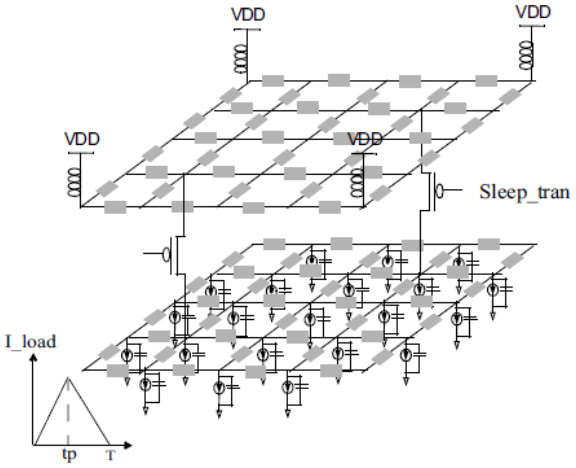

Figure 3. Power gating modeling

From the figure 3 it can be visualized as it consists two portions upper one is linear RL network and the lower one is linear RC network. By using constant voltage sources RL network can be excited where as in the RC network the excitation is with the time-varying current sources and it is because of the currents drawn from the logic circuits. With the triangle notation the current profiles can be modeled.

The entire system can be visualized as linear RLC network with the excitation from the voltage and current sources. This can be done with

replacement of vias where the sleep transistors are existed. In the ungated chips for power network analysis this technique is used widely. This can be overcome with the modified nodal analysis (MNA) formulation method. And it has the problem with non linearity of the network which exists because of the sleep transistors. With the inclusion of sleep transistors the circuits will be no longer linear. In the spice simulations by performing power gating noise analysis the above mentioned problem can be removed. While doing so the sleep transistors are turned ON and OFF to observe the voltage delivery behaviour.

The simplified power gating circuit can be modeled as shown in figure 4. It contains pull up and pull down gates with the virtual VDD and virtual Ground. the sleep transistors are connected into the necessary nodes with the specified ports for the power rails and inputs and outputs.

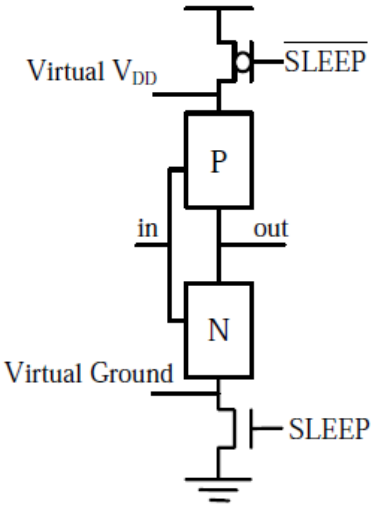

Figure 4: Power gating circuit.

The functionality of the circuit is same in the active state as the sleep transistor is in ON state. The overall phenomenon exists in the Standby mode. In this state the sleep transistor disconnects the gate from the ground as it turned into OFF state. Here care should be taken for achieving lower leakage current which can be obtained with the consideration of larger threshold voltage for the sleep transistors. Otherwise the sleep transistors will give high leakage current and causes the power gating less effective if the sleep transistor has the lesser threshold voltage. And also the additional power savings can be achieved with the lowering the width of the sleep transistor in compares to the total width of the pull-down network. For achieving power gating VTCMOS or Multi Threshold CMOS (MTCMOS) is used. The best practice for achieving higher power saving is using lower

threshold voltage transistors for the logic implementation and using higher threshold voltage transistors for the sleep transistors.

The expected amount of discharge current value can be obtained with the technique as shown in figure 4. The switching activity of the gate can be calculated as the ration of the multiplication product of the probability of the gate output at zero by the probability of the gate output at one. the switching activity of the gate would be accountable unless it leads to the negative impact of the design exists and causes increased sizes for the sleep transistors making the increased die size also the serious cause from increase of leakage and dynamic power and finally due to this clustered formation of gates produce worst case current discharges. By taking CLA adder typical parameters with the application of all the inputs concurrently to it can be reduced.

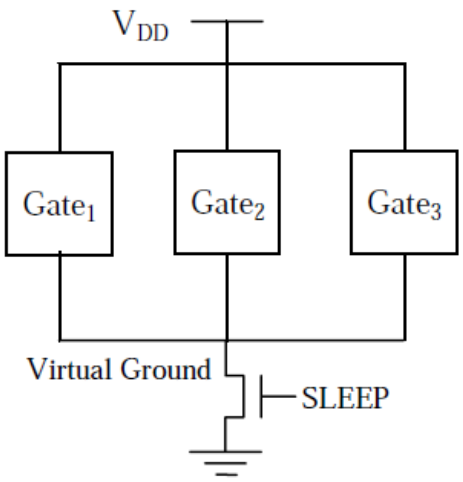

Figure 5: Using one sleep transistor for several gates.

In contrast to the usage of single sleep transistor for overall gate the sharing of sleep transistor for the circuit can be done by applying the above technique as shown in the figure 6.

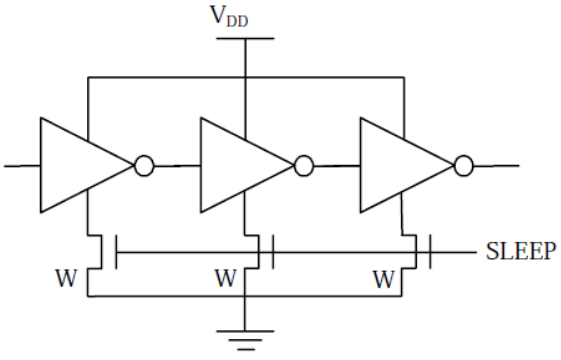

Figure 6: Sleep transistor sharing.

4. Leakage Control In Active Mode

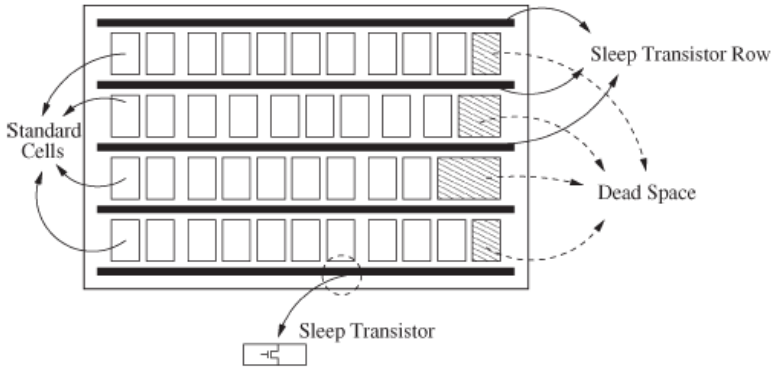

Figure 7. Proposed design methodology.

By using the techniques which were discussed earlier the domination of the leakage power compare to the overall power consumption of the circuit in Standby mode can be reduced. if that is not the case and the leakage power is minimum when compare to the overall power consumption the total power consumption is needs to taken into account where the combination of switching power dissipation and active mode leakage has to consider and thereby optimization of circuit is to be considered. And it can be achieved by considering the following techniques.

- Multiple Threshold Cells
- Long Channel Devices
- Minimum Leakage Vector Method
- Stack Effect-based Method
- Sizing with Simultaneous Threshold and Supply Voltage Assignment

The proposed clustering algorithm [8] used the approach of constrained minimization in which for the given timing constraints single cost function has taken. The iterative row selection scheme has used in the clustering algorithm. In the iterative row selection process all rows are selected in the initial stage and are marked as gated rows. in the next step the second row is taken and rows are progressively eliminated based on the given timing constraints until it reach the maximal set of rows where the leakage cost function can be minimized. The output of a gate is represented in the form of vectors for the discharging currents for the convenience of vector comparisons. And the same can be evaluated from the flow chart of the figure 8.

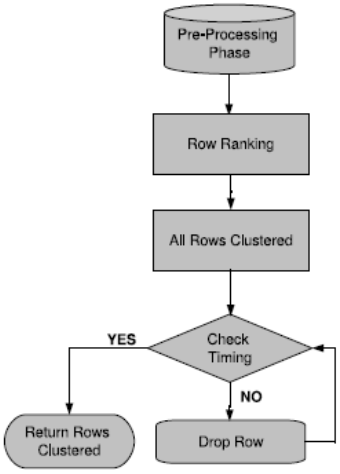

Figure 8: Clustering algorithm.

The proposed scheme [9] can be easily implemented to cope with the single set of sleep transistors. the load dependent delay di can be denoted mathematically as follows.

$$d^{i}\alpha \frac{C_L V_{dd}}{(V_{dd} - V_{tL})^{\alpha}} \tag{5}$$

And from the above equation the mathematical terms can be defined as the load capacitance for the CL and low voltage threshold is about 350 mV for the VtL and supply voltage Vdd is 1.8 V and α as the velocity saturation index and which is about 1.3 for the 180nm CMOS technology.

The propagation delay of a gate in presence of the sleep transistor can be expressed as

$$d_{sleep}^{i} = \frac{KC_L V_{dd}}{(V_{dd} - 2V_x - V_{tL})^{\alpha}} \tag{6}$$

And from the above equation the internal terminology is about Vx is for the virtual rails, K is the proportionality constant. And from the above equation the internal terminology is about Vx is for the virtual rails, K is the proportionality constant. The logic gates operates at the virtual supply rails about the magnitude of Vx from the supply rails on either side but not operates at the true supply rails (Vdd) in the active mode. From this can conclude that the effective supply voltage is Vdd-2Vx for the gate.

If the ON current of the sleep transistor in the active mode is IsleepON the sleep transistor will be in the linear region of operation. And by using the basic device equations the drain to source current of the sleep transistor in

the linear region for the sleep transistor can be denoted in the mathematical notation as

$$I_{sleep_{ON}} = \mu_n C_{ox}(W/L)_{sleep}((V_{dd} - V_{tH})V_x - \frac{V_x^2}{2}) \quad (7)$$

$$I_{sleep_{ON}} \approx \mu_n C_{ox}(W/L)_{sleep}(V_{dd} - V_{tH})V_x \quad (8)$$

And also the sleep transistor leakage current in the sleep mode can be identified with the mathematical expressions as follows

$$I_{leak} = \mu_n C_{ox}(W/L)_{sleep} e^{1.8} V_T^2 e^{\frac{V_{gs}-V_{tH}}{nV_T}} (1 - e^{\frac{-V_{ds}}{V_T}}) \quad (9)$$

From the above equation the terms can be represented as µn is the N-mobility, VT id the thermal voltage=26mV, VtH is the high threshold voltage and n is the subthreshold swing parameter. And from the above the relations between di sleep and Vx can be determined. By substituting the notations of di sleep, (W/L)sleep from the equations (4)-(7) the relationship between the leakage and delay can be denoted as follows

$$I_{leak} = \mu_n C_{ox} e^{1.8} V_T^2 e^{\frac{V_{gs}-V_{tH}}{nV_T}} (1 - e^{\frac{-V_{ds}}{V_T}}) \frac{I_{sleep_{ON}}}{\mu_n C_{ox}(V_{dd} - V_{tH})} \times \frac{d_{sleep}^{1/\alpha}}{(V_{dd} - V_{tL})d_{sleep}^{1/\alpha} - (KC_L V_{dd})^{1/\alpha}}. \quad (10)$$

For examine the power reduction techniques six standard benchmarks are taken into account as test benches. Those are 27 bit channel interrupt controller (CIC), 32 single error correcting circuit, a four bit ALU/Function Generator, 6 bit array multiplier design, 32 bit priority checker and finally 4 bit carry look ahead adder. These benchmarks provide the different fan outs for the different gates for offering variety of different circuits. CLA adder consists of 28 gates and all are designed and tested using 180 nm Technology.

Algorithm: *Time_Frame_Partitioning*(*MIC*(C_i,T_j), *n*)

```
1: Output: An efficient partitioning
2: /* step 1: mark the candidate time units */
3: for j ← 1 to NUM_TF do
4:     if (the n+1 largest MIC(C_i) occurs in T_j) then
5:         mark(T_j);
6:     end if
7: end for
8: /* step 2: n-way partitioning */
9: use n cuts to separate the marked T_j;
10: return
```

Figure 8. Variable length n-way partitioning algorithm.

5. Simulation Results

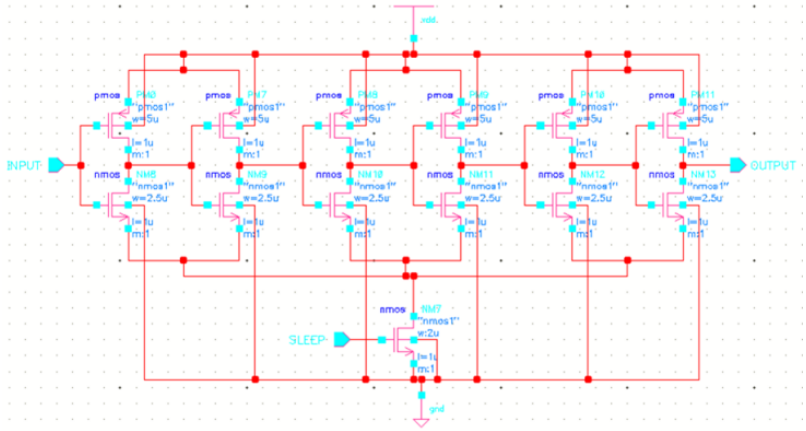

Figure 9. Sleep transistor model 1

From the figures 1, 2 and 9 it can be concluded that the virtual ground line actually help reduce the ground bounce which were adjoined by the wire and junction capacitance acts as reservoir for current or local charge sink. To reduce the offset effects of the sleep transistors if taken lower sized sleep transistor by taking the extreme high value of capacitance. Where the RC network will do the low pass filtering action and here it should meet the value as large for the RC time constant in order to make the virtual ground to the fraction of peak dc value.

Two constraints are needed to be considered for the ground bounce by simultaneously reducing the dynamic and leakage power with first constraint of maintaining the speed degradation to 5% and second constraint as ground bounce never exceed to 50 mv. These two constraints are sufficient to make the circuit for achieving speed and noise margins.

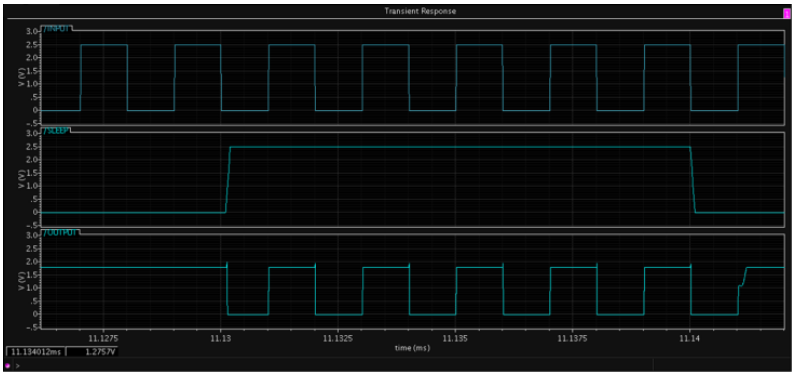

Figure 10. Output wave forms of sleep transistor

For scaling down the devices there are two mechanisms are existed viz. sub threshold leakage and gate leakage. Unfortunately with the increase of the technology scaling the sub threshold leakage and gate leakage would

increase rapidly. Decaps made up of gate oxide MOS transistors with the long wide channels are used for getting the large capacitance.

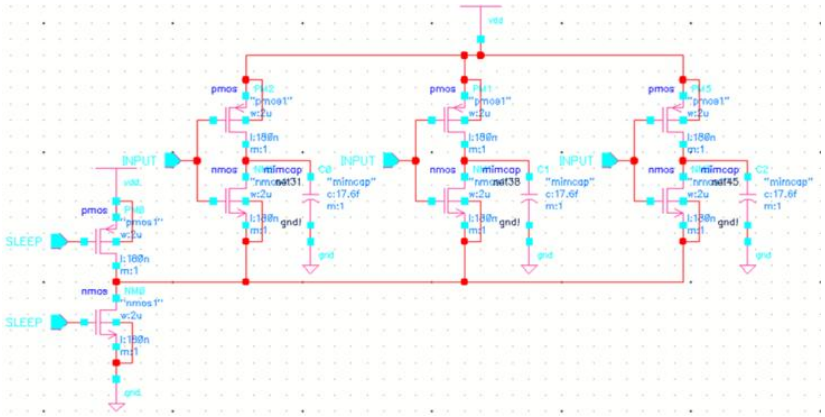

Figure 11. Sleep transistor model 2

Due to the continuous switching of the core logic and I/O buffers power grid noise will exist and this power gating noise is because of the switching action on and off of the sleep transistors.

From the above analysis the discharge current can be expected. Based on the multiplication value of the probability of the gate will be at zero to the probability of the gate will be at one gives the switching activity of the gate.

6. CONCLUSIONS

The clustered sleep transistors leakage power reduction techniques has analyzed and discussed various advantages and improvements need to take for the advancements of the sleep transistors for achieving the higher power saving and for using maximum die area with the consideration of the various algorithms proposed by the different designers which are considering as the standard designs. And all are designed and tested with 180 nm technology by using the spice simulation. And the research has to be done on the power scaling of the sleep transistors in the standby mode for the better performance.

7. ACKNOWLEDGMENTS

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REFERENCES

[1] Sathanur, Ashoka, et al. *Row-based power-gating: a novel sleep transistor insertion methodology for leakage power optimization in nanometer cmos circuits*. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 19, No. 3, 2011, pp. 469-482.

[2] Homayoun, Houman, et al. *MZZ-HVS: multiple sleep modes zig-zag horizontal and vertical sleep transistor sharing to reduce leakage power in on-chip SRAM peripheral circuits.* IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 19, No. 12, 2011, pp. 2303-2316.

[3] V. Khandelwal and A. Srivastava. *Leakage control through fine-grained placement and sizing of sleep transistors*. In Proc. IEEE/ACM Int. Conf. CAD (ICCAD), San Jose, CA, Nov. 2004, pp. 533–536.

[4] J. Kao, A. Chandrakasan, and S. Narendra. *MTCMOS hierarchical sizing based on mutual exclusive discharge patterns*. In Proc. ACM/ IEEE Des. Autom. Conf. (DAC), San Francisco, CA, Jun. 1998, pp. 495–500.

[5] S. Mutoh, S. Shigematsu, Y. Matsuya, H. Fukuda, and T. Kaneko. *1-V power supply high-speed digital circuit technology with multithreshold voltage CMOS*. J. Solid-State Circuits, vol. 30, no. 8, pp. 847–854, Aug. 1995.

[6] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand. *Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOScircuits*. Proc. IEEE, vol. 91, no. 2, pp. 305–327, Feb. 2003.

[7] M. Keating, D. Flynn, R. Aitken, A. Gibbons, and K. Shi. *Low Power Methodology Manual: For System-on-Chip Design*. New York: Springer, 2007.

[8] H. Jiang, M. Marek-Sadowska, and S. R. Nassif. *Benefits and costs of power-gating technique*. In Proc. IEEE Int. Conf. Comput. Des.(ICCD), San Jose, CA, Oct. 2005, pp. 559–566.

[9] M. Anis, S. Areibi, and M. Elmasry. *Design and optimization of multithreshold CMOS (MTCMOS) circuits*. IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., Vol. 22, No. 10, pp. 1324–1342, Oct. 2003.

[10] J. Kao, A. Chandrakasan, and D. Antoniadis. *Transistor sizing issues and tool for multi-threshold CMOS technology*. In Proc. ACM/IEEE Des. Autom. Conf. (DAC), Anaheim, CA, Jun. 1997, pp. 409–414.

[11] F. Fallah and M. Pedram. *Standby and active leakage current control and minimization in CMOS VLSI circuits*. IEICE Trans. Electron., Vol. E88-C, No. 4, pp. 509–519, Apr. 2005.

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